L Number	Hits	Search Text	DB	Time stamp
1	98839	semiconductor and gate and source and drain	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/10/04 13:59
2	70189	(semiconductor and gate and source and drain) and substrate	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/10/04 14:00
3	36144	((semiconductor and gate and source and drain) and substrate) and well	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/10/04 14:01
4	13093	(((semiconductor and gate and source and drain) and substrate) and well) and input and output	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/10/04 14:02
5	2098	((((semiconductor and gate and source and drain) and substrate) and well) and input and output) and (contact adj hole)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/10/04 14:03
6	505	(((((semiconductor and gate and source and drain) and substrate) and well) and input and output) and (contact adj hole)) and nand	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/10/04 14:10
7	445	(((((semiconductor and gate and source and drain) and substrate) and well) and input and output) and (contact adj hole)) and "and"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/10/04 14:10
8	575	(((((semiconductor and gate and source and drain) and substrate) and well) and input and output) and (contact adj hole)) and nor	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/10/04 14:11
9	222	(((((semiconductor and gate and source and drain) and substrate) and well) and input and output) and (contact adj hole)) and "or"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/10/04 14:11

L Number	Hits	Search Text	DB	Time stamp
1	46145	semiconductor and cmos	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/10/04 14:34
2	1444	(semiconductor and cmos) and ((well or substrate) adj contact)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/10/04 14:36
3	1710	(semiconductor and cmos) and ((well or substrate or body) adj contact)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/10/04 14:38
4	504	((semiconductor and cmos) and ((well or substrate or body) adj contact)) and (contact adj hole)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/10/04 14:39
5	35	(((semiconductor and cmos) and ((well or substrate or body) adj contact)) and (contact adj hole)) and nand	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/10/04 15:08
6	63	(((semiconductor and cmos) and ((well or substrate or body) adj contact)) and (contact adj hole)) and nor	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/10/04 15:31
7	55	(((semiconductor and cmos) and ((well or substrate or body) adj contact)) and (contact adj hole)) and "and"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/10/04 15:42
8	18	(((semiconductor and cmos) and ((well or substrate or body) adj contact)) and (contact adj hole)) and "or"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/10/04 15:48

WEST

End of Result Set

Generate Collection Print

L1: Entry 1 of 1 File: JPAB Aug 9, 1996

PUB-NO: JP408204140A
DOCUMENT-IDENTIFIER: JP 08204140 A
TITLE: SILICON-ON-INSULATOR SEMICONDUCTOR DEVICE AND BIAS VOLTAGE GENERATING CIRCUIT

PUBN-DATE: August 9, 1996

INVENTOR-INFORMATION:

NAME	COUNTRY
OKUMURA, KOICHIRO	
KUROSAWA, SUSUMU	

ASSIGNEE-INFORMATION:

NAME	COUNTRY
NEC CORP	

APPL-NO: JP07031348
APPL-DATE: January 27, 1995

INT-CL (IPC): H01 L 27/04; H01 L 21/822; H01 L 21/8238; H01 L 27/092; H01 L 27/108; H01 L 21/8242; H01 L 27/12; H01 L 29/78; H01 L 29/786; H01 L 21/336

ABSTRACT:

PURPOSE: To operate a semiconductor device rapidly in the active time while reducing power consumption in the stand-by time by controlling the threshold voltage changing the bias of base substance in the active time and stand-by time.

CONSTITUTION: P type silicon base substance of NMOS formed on a silicon-on- insulator substrate is impressed with a voltage higher than the earth potential in the active time and the voltage lower than the normal directional voltage VF in the PN junction. Next, in the case of stand-by time, as for the earth potential, likewise, PMOS type silicon base substance 106 is impressed with a voltage lower than power supply voltage VDD in case the of active time and higher than the voltage reduced by the normal directional voltage of PN junction from the power supply voltage VDD while VDD in the stand-by time thereby enabling the absolute threshold voltage of MOS type FET in the active time lower than that in the stand-by time.